FIR Filter Design

Project 2 CE6325 VLSI DESIGN: SYNOPSYS PROJECT

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Fall 2024

**Project Description:**

The Finite Impulse Response (FIR) filter designed in Project 1 had to be scaled to reach the project specifications. The original design had 386 cells after analysis and elaboration using Synopsys EDA tool.

The filter tap (order) was changed to 15 and both the input (Data\_in) and output (Data\_out) sizes were increased. These changes increased the latency in the simulation. To improve this, Pipeline registers were added to the output of each Multiply node and input of each addition node to reduce latency and idle time.

**Design Specification:**

Filter order: 15

Filter coefficients: [7, 8, 9, 12, 4, 7, 8, 9, 12, 4]

Data\_in size: 8

Data\_out size: 20

PR\_mul and PR\_add: Pipeline registers for multiplication results and addition results respectively

**Data flow of the Design**

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Figure1: Finite Impulse Response (FIR) Filter using Multiply and Accumulate with Pipeline Registers

**Testbench Process Flow**

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Figure 2: Shows the Testbench Process flow

Table 1 showing Filter out with when Data\_in = decimal (6) in this case



Table 1 shows that Data\_in will go shift through all of Sample[k] when enough time is allowed before changing the value at the input. The value in each register of Sample[k] is multiplied by the filter

**Design Simulation Results from Behavioral Model**

**Netlist from Verilog Model using Intel Quartus Prime and Questa**

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Figure 3: Netlist for the FIR filter

Table2 shows the observed values from the Behavioral Model Transcript Report

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**Simulation Waveform for the Behavioral Model using Intel Quartus Prime and Questa**

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Figure 4: Behavioral Waveform showing that that the Data\_out is dependent on reset and rising edge of the clock signal.

**Design Simulation Results from Structural Model**

Table3 shows the observed values from the Structural Model Transcript Report which is identical to behavioral Model’s Trancript report

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**Simulation Waveform for the Structural model**

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Figure 5: Structural Waveform showing that that the Data\_out is dependent on reset and rising edge of the clock signal.

**Cell Report from Synopsys (note some of the cells have been deleted)**

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**Header.v module (contains all the different cell types use to create the structural Model)**

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Summary:

The initial design from Project1 had to be scaled to meet the project Specification of at least 3000 cells

The structural Model from Synopsys and the header file were simulated on Model sim to obtain the transcript report and the waveform

The Table from the behavioral model was identical to the table from the structural model, the waveforms are also identical. These concludes that the structural model and the behavioral model are identical

The header.v file shows the different types of cells (inv, nan2, nan3, aoi12, oai12, dff, etc.) that will be need in the design library to create the FIR filter

The design will have a total of 3694 cells.